a data-input circuit which latches data signals in response to a strobe signal, and outputs the data signals in response to the clock signal;

an internal circuit which writes the data signals supplied from the data-input circuit in memory cells indicated by the address signals supplied from the address-input circuit; and

a bypass circuit provided in parallel to said delay circuit, wherein the address signals pass through the bypass circuit and bypass said delay circuit in a data-read mode.

5

44. A memory circuit, comprising:

an address-input circuit which latches address signals in response to a clock signal, and outputs the address signals in response to a strobe signal, the address-input circuit includes a delay circuit which operates in response to a clock signal;

a data-input circuit which latches data signals in response to a strobe signal, and outputs the data signals in response to the strobe signal;

an internal circuit which writes the data signals supplied from the data-input circuit in memory cells indicated by the address signals supplied from the address-input circuit; and

a bypass circuit provided in parallel to said delay circuit, wherein the address signals pass through the bypass circuit and bypass said delay circuit in a data-read mode.